What is claimed is:

1. A method of etching an opening through a layer of dielectric, comprising the steps of:

providing a semiconductor substrate, said substrate having been provided with points of electrical contact in or on the surface thereof;

depositing a layer of dielectric over the surface of the substrate;

creating a patterned and developed layer of photoresist over the surface of said layer of dielectric, creating an opening through said layer of photoresist, exposing the surface of said layer of dielectric through said opening;

etching said exposed surface of said layer of dielectric in accordance with said opening created in said layer of photoresist, by applying anisotropic, RIE processing, using as etchant gas a mixture of CF_4 + CHF_3 + O_2, whereby said CF_4 + O_2 is provided at a flow rate of about 15 sccm, whereby the flow rate of the CHF_3 is between about 10 and 200 sccm, a temperature in excess of 120 degrees C. and preferably in the range between 120 and 200 degrees C. and more preferably about 150 degrees C., a gas pressure between about 200 and 800 mTorr and more preferably about 500 mTorr, rf power density about 400 Watts, no magnetic field applied, time of the etch between about 5 and 50 seconds and more preferably about 25 seconds, creating an opening through

said layer of dielectric having sidewalls intersecting with the surface of said substrate under an angle of about 60 degrees; and

removing said patterned and developed layer of photoresist from the surface of said layer of dielectric.

2. The method of claim 1, the flow rate of the CHF_3 being between about 90 and 170 sccm, creating an opening through said layer of dielectric having sidewalls intersecting with the surface of said substrate under an angle of about 45 degrees.

3. The method of claim 1, the flow rate of the CHF_3 being between about 170 and 250 sccm, creating an opening through said layer of dielectric having sidewalls intersecting with the surface of said substrate under an angle of about 30 degrees.

4. The method of claim 1, the flow rate of the CHF_3 being between about 10 and 300 sccm.

5. The method of claim 1 with additional steps of:

depositing a layer of metal over the surface of said layer of dielectric, including the opening created in said layer of dielectric; and

removing excess metal from the surface of the layer of dielectric, leaving a metal plug in place filing said opening created in said layer of dielectric.

6. The method of claim 5 with an additional step being performed prior to said depositing a layer of metal over the surface of said layer of dielectric, said additional step comprising deposition a layer of barrier material or a layer of seed material over the surface of the layer of dielectric.

7. A method for providing a plurality of conductive metallization patterns, separated by insulating layers, on the surface of an integrated circuit, comprising the steps of:

providing a semiconductor substrate having a surface, conductive points of electrical contact having been provided in or on the surface of said substrate;

depositing a first layer of dielectric over the surface of said substrate, including the surface of said conductive points of electrical contact;

first patterning and etching said first layer of dielectric, creating a first openings in said first layer of dielectric, said first openings having sloping sidewalls, said first patterning and etching comprising applying anisotropic RIE etch using a mixture of CF_4 + CHF_3 + O_2 as etchant gasses;

filling said first openings created in said first layer of dielectric with a first metal, removing excess metal from the surface of said first layer of dielectric, creating first metal plugs in said first layer of dielectric, said first metal plugs having a first surface area;

depositing a second layer of dielectric over the surface of said first layer of dielectric, including the surface of said first metal plugs created in said first layer of dielectric;

depositing an etch stop layer of the surface of said second layer of dielectric;

patterning and etching said etch stop layer, creating openings in said etch stop layer that align with said first metal plugs created in said first layer of dielectric, exposing the surface of said second layer of dielectric, said openings in said etch stop layer having a surface area that is smaller than said first surface area of said first metal plugs by a measurable amount;

depositing a third layer of dielectric over the surface of said etch stop layer, including the exposed surface of said second layer of dielectric;

depositing a layer of photoresist over the surface of said third layer of dielectric, patterning and developing said layer of photoresist, creating openings in said layer of photoresist that align with said first surface area of said first metal plugs

created in said first layer of dielectric, said openings in said layer of photoresist having a surface area that is about equal to said first surface area;

second etching said third layer of dielectric in accordance with said openings created in said layer of photoresist, said second etch further extending through said second layer of dielectric in accordance with said openings created in said etch stop layer, said second etch comprising applying anisotropic RIE etch to said third and said second layer of dielectric using a mixture of CF_4 + CHF_3 + O_2 as etchant gasses, creating a second opening in said third layer of dielectric having sloping sidewalls in addition to creating a third opening through said second layer of dielectric having sloping sidewalls, exposing the surface of said first metal plugs;

removing said patterned layer of photoresist from the surface of said third layer of dielectric, exposing the surface of said third layer of dielectric;

depositing a barrier layer over sidewalls of said second openings in said third layer of dielectric, including over sidewalls of said third openings created in said second layer of dielectric, including over said exposed surface of said first metal plugs, including over said exposed surface of said third layer of dielectric;

depositing a layer of conductive material over the surface of said barrier layer; and

removing excess conductive material from above the surface of said third layer of dielectric, further removing said barrier layer from above the surface of said third layer of dielectric, leaving said barrier layer and said conductive material in said second openings in said third layer of dielectric and in said third openings in said second layer of dielectric.

8. The method of claim 7 with an additional step of depositing a seed layer over the surface of said barrier layer, said additional step being performed after said depositing a barrier layer, said additional step being followed by steps of:

depositing a layer of conductive material over the surface of said seed layer; and

removing excess conductive material from above the surface of said third layer of dielectric, further removing said barrier layer and said seed from above the surface of said third layer of dielectric, leaving said barrier layer and said seed layer and said conductive material in said second openings in said third layer of dielectric and in said second openings in said second layer of dielectric.

9. The method of claim 7, said first etch stop layer comprising silicon nitride.

10. The method of claim 7, said first metal plugs comprising copper.

11. The method of claim 7, said layer of conductive material deposited over the surface of said barrier layer comprising copper.

12. The method of claim 8, said layer of conductive material deposited over the surface of said seed layer comprising copper.

13. The method of claim 8, said seed layer comprising copper.

14. The method of claim 7, said barrier layer comprising titanium nitride.

15. The method of claim 7, said depositing a layer of conductive material over the surface of said seed layer comprising methods of Electro Chemical Plating (ECP).

16. The method of claim 8, said depositing a layer of conductive material over the surface of said seed layer comprising methods of Electro Chemical Plating (ECP).

17. The method of claim 7 wherein said first patterning and etching said first layer of dielectric is applying anisotropic, RIE processing, using as etchant gas CF_4 + CHF_3 + O_2, a flow rate of CHF_3 being between about 10 and 200 sccm, at a temperature in excess of 120 degrees C. and preferably in the range between 120 and 200 degrees C. and more preferably about 150 degrees C., at a gas pressure between about 200 and 800 mTorr and more preferably about 500 mTorr, with an rf power density about 400 Watts, with no magnetic field applied, with a time of the first etch between about 5 and 50 seconds and more preferably about 25 seconds.

18. The method of claim 7 wherein said second etching said third layer of dielectric extending through said second layer of dielectric is applying anisotropic, RIE processing, using as etchant gas CF_4 + CHF_3 + O_2, a flow rate of CHF_3 being between about 10 and 200 sccm, at a temperature in excess of 120 degrees C. and preferably in the range between 120 and 200 degrees C. and more preferably about 150 degrees C., at a gas pressure between about 200 and 800 mTorr and more preferably about 500 mTorr, with an rf power density about 400 Watts, with no magnetic field

applied, with a time of the first etch between about 5 and 50 seconds and more preferably about 25 seconds.

19. A multilayer integrated circuit structure, comprising:

a semiconductor substrate having a surface, a plurality of semiconductor devices having been provided in or on the surface of said substrate, further conductive points of electrical contact having been provided in or on the surface of said substrate;

first metal plugs being provided on the surface of the substrate, said first metal plugs being imbedded in a first layer of dielectric deposited over the surface of said substrate, said first metal plugs being aligned with said conductive points of electrical contact having been provided in or on the surface of said substrate, said first metal plugs having a surface comprising a first surface area and a therein centrally located second surface area, said second surface being smaller than said first surface by a measurable amount;

a second layer of dielectric deposited over the surface of said first layer of dielectric, including the surface of said first metal plugs;

an etch stop layer deposited of the surface of said second layer of dielectric, said etch stop layer having been patterned and etched, creating openings in said etch stop layer that align

with said second surface area of said first metal plugs, exposing the surface of said first layer of dielectric, said openings in said etch stop layer having a surface area that is about equal to said second surface area of said first metal plugs;

a third layer of dielectric deposited over the surface of said etch stop layer, including the exposed surface of said second layer of dielectric;

first openings created in said third layer of dielectric, said first openings having sloping sidewalls, said first openings in said third layer of dielectric having a surface area that is about equal to said first surface area of said first metal plugs, said first openings in said third layer of dielectric extending to said openings created in said layer of etch stop;

second openings created in said second layer of dielectric, said second openings having sloping sidewalls, said second openings in said second layer of dielectric extending from said openings created in said layer of etch stop to said second surface of said first metal plugs;

a barrier layer deposited over sidewalls of said first openings in said third layer of dielectric, over said second openings in said second layer of dielectric, over said second surface of said first metal plugs; and

a layer of conductive material deposited over the surface of said barrier layer, excess conductive material having been

removed from above the surface of said third layer of dielectric, furthermore said barrier layer having been removed from above the surface of said second layer of dielectric.

20. The structure of claim 19, with the addition of a seed layer deposited over the surface of said barrier layer, said seed layer equally having been removed from above the surface of said second layer of dielectric.

21. The structure of claim 19, said conductive points of electrical contact having been provided in or on the surface of said substrate comprising copper.

22. The structure of claim 19, said layer of conductive material deposited over the surface of said barrier layer comprising copper.

23. The structure of claim 20, said seed layer comprising copper.

24. A method for providing a plurality of conductive metallization patterns separated by insulating layers on the surface of an integrated circuit, comprising the steps of:

providing a semiconductor substrate having a surface, said substrate having been provided with a multiplicity of semiconductor devices in or on the surface thereof;

first metal plugs being provided on the surface of the substrate, said first metal plugs being imbedded in a first layer of dielectric deposited over the surface of said substrate, said first metal plugs being aligned with said conductive points of electrical contact having been provided in or on the surface of said substrate, said first metal plugs having a surface comprising a first surface area and a therein centrally located second surface area, said second surface being smaller than said first surface by a measurable amount, said first metal plugs having been created using control chemistry creating sloping sidewalls of said first metal plugs;

depositing a second layer of dielectric over the surface of said first layer of dielectric, followed by depositing an etch stop layer over the surface of said second layer of dielectric, followed by depositing a third layer of dielectric over the surface of said etch stop layer;

patterning and etching said third layer of dielectric, said etch stop layer and said second layer of dielectric, creating openings through said third layer of dielectric, said etch stop layer and said second layer of dielectric, said openings aligning with said first metal plugs being provided on the surface of the

substrate, said etching using control chemistry creating sloping sidewalls of said openings created in said third layer of dielectric, said etch stop layer and said second layer of dielectric;

depositing a barrier layer over inside surfaces of said openings created in said third layer of dielectric, said etch stop layer and said second layer of dielectric, including the surface of said third layer of dielectric;

depositing a seed layer over the surface of said barrier layer;

depositing a layer of conductive material over the surface of said seed layer; and

removing excess conductive material from above the surface of said second layer of dielectric.

25. The method of claim 24, said conductive points of electrical contact having been provided in or on the surface of said substrate comprising copper.

26. The method of claim 24, said layer of conductive material deposited over the surface of said seed layer comprising copper.

27. The method of claim 24, said seed layer comprising copper.

28. The method of claim 24, said barrier layer comprising titanium nitride.

29. The method of claim 24, said first metal plugs comprising copper.

30. The method of claim 24, said control chemistry used in creating sloping sidewalls of said first metal plugs comprising applying anisotropic RIE etch using a mixture of CF_4 + CHF_3 + O_2 as etchant gasses.

31. The method of claim 24, said using control chemistry creating sloping sidewalls of said openings created in said third layer of dielectric, said etch stop layer and said second layer of dielectric comprising applying anisotropic RIE etch using a mixture of CF_4 + CHF_3 + O_2 as etchant gasses.